What Is Claimed Is:

1. A method of fabricating a semiconductor device comprising:

forming a trench in a substrate;

forming a gate electrode by depositing and planarizing an oxide layer and polysilicon on the substrate including the trench;

forming a gate oxide layer and a polysilicon layer on the substrate and the gate electrode;

forming a source region and a drain region by a photo process; and

forming a contact plug on at least one of the source region and the drain region.

2. A method as defined in claim 1, wherein forming the trench comprises performing anisotropic etching using Cl_2 and HBr as etching gas.

3. A method as defined in claim 1, wherein forming the gate electrode by depositing and planarizing the oxide layer and the polysilicon comprises forming the polysilicon by LPCVD.

4. A method as defined in claim 1, wherein forming the gate electrode by depositing and planarizing the oxide layer and the polysilicon comprises performing CMP until a surface of the substrate is exposed.

5. A method as defined in claim 1, wherein forming the gate oxide layer and the polysilicon layer on the substrate and the gate electrode

comprises forming the polysilicon layer by LPCVD.

6. A method as defined in claims 5, wherein the LPCVD is performed at a temperature of about 420-520°C using a Si_2H_6 gas.

7. A method as defined in claims 3, wherein the LPCVD is performed at a temperature of about 420-520°C using a Si_2H_6 gas.

8. A method as defined in claim 1, wherein the gap between the source and the drain is controlled by a gap between photoresist patterns.

9. A method as defined in claim 1, wherein the gate oxide layer comprises a USG layer based on TEOS.

10. A method as defined in claim 1, wherein forming the gate oxide layer comprises performing HDP CVD.

11. A method as defined in 1; wherein the gate oxide layer comprises a USG layer formed at a high temperature.

12. A semiconductor device comprising:

a trench in a substrate;

a gate electrode buried inside the trench;

a gate oxide layer on the gate electrode;

a polysilicon layer on the gate oxide layer;

source and drain regions in the polysilicon layer;

an interlayer dielectric on the polysilicon layer; and

a contact plug in the interlayer dielectric and contacting one of the source and the drain.

13. A semiconductor device as defined in claim 12, wherein the trench is formed by anisotropic etching using Cl_2 and HBr as etching gas.